Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. An erasable programmable read only memory that omits a control gate comprising:

a doped region formed by ion implantation in a substrate;

a first conductive area covered on said substrate and forms a first cross structure with a first overlap area to acts as a select transistor gate and connected to a select gate voltage (V_{SG});

a second conductive region located at a side of said first conductive region and on said substrate and forms a second cross structure with a second overlap area to acts as a floating gate;

wherein a feature of said erasable programmable read only memory is that a control gate is omitted, thereby reducing device size and integratable with CMOS process.

[c2] 2.The erasable programmable read only memory of Claim 1 wherein during a mode for writing "digital one", a selected word line is grounded and a unselected word line is bias to about a first voltage, wherein a selected bit

line is grounded, a unselected bit line is about said first voltage, a source node and a N well are connected to said first voltage, thereby turning on said selected transistor and injecting hot channel carrier onto said floating gate of said second P-type metal-oxide semiconductor transistor.

[c3] 3.The erasable programmable read only memory of Claim 1 wherein during a mode for writing "digital zero", a selected word line is grounded and a unselect word line is applied to a second voltages, a selected bit line is about said first second voltage and a unselect bit line is also about said second voltage, a source node and a N well are respectively connected to said second voltage, thereby turning off said select transistor and hot carrier is unable to inject onto said floating gate.

[c4] 4.The erasable programmable read only memory of Claim 1 wherein during read mode, a selected word line is grounded and unselected word line is biased to a third voltages, a selected bit line is about a forth voltage, a unselect bit line is biased to said third voltage, a source node is also bias to said third voltage and a N well is connected to said third voltage, thereby turning on said select transistor for reading the status stored in said floating gate.

[c5] 5.The erasable programmable read only memory of Claim 1 wherein a cell array, an unselect transistor does not suffer a drain disturbance because said unselect transistor is at off-state and the electric field between said bit line and said floating gate is not strong enough to inject/generate hot carriers, a coupling of said floating gate is not induced by the word line, thereby eliminating the gate disturbance phenomenon.

[c6] 6. A P-channel single-poly memory unit comprising:
a P-type metal-oxide-semiconductor (PMOS) select transistor formed on an N-well of a substrate, wherein said PMOS select transistor has a first P-doped source region, a control gate electrode, and a first P-doped drain region, and wherein said first P-doped source region and said first P-doped drain region defines a first P-channel under said control gate electrode; and
a single-poly PMOS memory cell formed on said N-well, wherein said single-poly PMOS memory cell has a floating gate, a second P-doped drain region and said first P-doped drain region of said PMOS select transistor serves as a second P-doped source region of said single-poly PMOS memory cell, and wherein said second P-doped source region and said second P-doped drain region defines a second P-channel under said floating gate.

[c7] 7. The P-channel single-poly memory unit of claim 6 wherein there is no control gate located on said floating gate of said single-poly PMOS memory cell.

[c8] 8. The P-channel single-poly memory unit of claim 6 wherein during a programming operation a well voltage is applied to said N-well, a first voltage that is less than said well voltage is applied to said second P-doped drain region of said single-poly PMOS memory cell, thereby coupling a second voltage on said floating gate to turn on said second P-channel.